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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,527	10/02/2000	Chung-Lung Kevin Shum	POU9-2000-0163US1	4322
7590	09/02/2004		EXAMINER	
Troy J LaMontagne Cantor Colburn LLP 55 Griffin Road South Bloomfield, CT 06002			ROSS, JOHN M	
			ART UNIT	PAPER NUMBER
			2188	6
			DATE MAILED: 09/02/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/677,527	SHUM ET AL.
	Examiner	Art Unit
	John M Ross	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 July 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-35 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7,9-26 and 28-35 is/are rejected.
 7) Claim(s) 8 and 27 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 18 December 2000 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Status of Claims

1. Claims 2-4, 20-21 and 23 are amended.

Claims 1-35 are pending in the application.

Claims 1-7, 9-26 and 28-35 are rejected.

Claims 8 and 27 are objected to.

Response to Amendment

2. Applicant's amendments and arguments filed on 8 July 2004 (Paper No. 5) in response to the Office Action mailed on 8 April 2004 have been fully considered but they are not persuasive. Therefore, the rejections maintained from the previous Office Action are restated below.

Specification

3. The amendment has overcome the objection to the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-4 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821) and Anderson (US 3,735,360).

As in claims 1-4, and 16-17 APA discloses a conventional multi-processor computer system comprising a plurality of central processing units each including an execution unit, an instruction unit, and a plurality of caches including separate instruction and operand caches, where the central processing units are connected to a shared main memory through a storage controller (Page 1, lines 5-22). It is noted that an existing system cache coherency protocol and cache handling requirements employed by the storage controller are inherent in the system of APA in order to maintain consistency of the shared data between the caches in the processors.

APA does not teach subjecting the instruction and operand caches to a cache coherency protocol with interlocks on cache block access, nor does APA teach the particular cache coherency protocol as required by claim 1.

APA also does not teach that the instruction and operand cache coherency protocol operates in cooperation with the existing cache coherency protocol and cache handling requirements as required by claims 2-4.

APA also does not teach shared read status, exclusive status and read-only status as required by claims 13-15.

Gaskins teaches a system comprising separate code (i.e. instruction) and data (i.e. operand) caches supporting self-modifying code by subjecting the code and data caches to a cache coherency protocol with interlocks on cache block access (Fig. 6, elements 605 and 607; column 6, line 64 to column 7, line 15; column 9, lines 19-24).

Anderson teaches a system comprising a pair of parallel and independent caches subjected to a cache coherency protocol (Fig. 1, elements 10, 15 and 16; column 5, lines 18-26), where a cache can have the only copy of a block of data (i.e. exclusive) or one of multiple copies of a block of data (i.e. shared), indicated by a fetch-only bit (Fig. 3, element 62; column 8, lines 10-21) in the cache directory (Fig. 3, element 27; column 5, lines 46-49).

Anderson further describes that when the block of data has exclusive status in a cache, the block may be stored into (i.e. written), but when the block of data is shared it may only be read (Column 8, lines 22-35). This latter state corresponds to a read-only status. Anderson further emphasizes that before a block of data can be stored into, other existing copies must be invalidated and exclusive ownership must be obtained (Column 8, lines 35-39).

Therefore, the protocol described by Anderson may be summarized as:

allowing shared read access by a first cache and second cache to a cache block if the cache block has read-only status in the first cache and the second cache;

allowing read and write access by the first cache and preventing access by the second cache to the cache block if the cache block has exclusive status in the first cache; and

interlocking write access to the cache block by the first cache with exclusive status if the cache block has read-only status in the second cache;

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to subject the instruction and operand caches to a cache coherency protocol with interlocks on cache block access as taught by Gaskins, in the system of APA, in order to support self-modifying code as taught by Gaskins.

Further regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol taught by Anderson, in the system made obvious by the combination of APA and Gaskins, due to the similarity in nature of the problems, namely to provide coherency between a pair of parallel caches sharing a common main storage where the same information may be stored in either cache.

Regarding claims 2-4, although the combination of APA, Gaskins and Anderson does not explicitly teach the instruction and operand cache coherency protocol operate in cooperation with the existing cache coherency protocol and cache handling requirements, Examiner takes Official Notice that it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to do so. As noted above, APA teaches a system with an existing cache coherency

protocol and cache handling requirements that allow a plurality of central processing units to share access to a main memory. As also noted above, the combination of APA, Gaskins and Anderson teaches a cache coherency protocol for maintaining consistency between an instruction and operand cache within the central processing units of APA. One skilled in the art would recognize that the first protocol does not preclude the second, and that both would be necessary for the system to properly function.

Claims 13-15 are rejected using the same rationale as for the rejection of claim 1, noting the teachings regarding shared, exclusive and read-only status contemplated by Anderson.

6. Claims 5-7, 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821) and Anderson (US 3,735,360) as applied to claim 3 above, and further in view of Mahalingaiah (US 6,073,217).

APA, Gaskins and Anderson are relied upon for the teachings relative to claim 3 as above.

As in claim 5, Gaskins further teaches that when an instruction fetch is requested, providing the instruction cache read-only status for a requested cache block (Fig. 2, element 205; column 2, lines 18-20; Fig. 8; column 8, lines 58-61), where it is readily apparent from Gaskins that the status for a block in the instruction cache must be read-only because the control unit (i.e.

instruction unit) (Fig. 2, element 222) may only fetch instructions and maintains them prior to execution (Column 2, lines 18-27).

Also as in claim 5, Anderson further teaches that when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in a first cache (Fig. 2; column 8, line 55 to column 9, line 3) and a request for exclusive status is transmitted to a storage control unit and a cross-interrogate signal is transmitted to a second cache (Fig. 2; column 9, lines 4-19).

The rationale derived from Anderson in the rejection of claim 3 above is incorporated herein for the teaching of storing in the first cache after exclusive status is obtained via the storage control unit following a response from the cross interrogation.

As in the rejection of claim 3 above, it is noted that the protocol applied to the first and second caches in Anderson is applied to the operand and instruction cache.

The combination of APA, Gaskins and Anderson does not teach the following steps as required by claim 5-6 and 9, however, these steps are taught by Mahalingaiah:

buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);

discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);

discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 41-59; column 9, lines 48-60); and

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15; column 8, lines 41-59).

Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column 5, lines 54-58).

Regarding claims 5-6 and 9, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated above, in the system made obvious by the combination of APA, Gaskins and Anderson, in order to allow correct execution of self-modifying code as taught by Mahalingaiah.

As in claim 7, Anderson further teaches that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated (Column 8, lines 35-39; column 9, lines 20-32).

As in claims 11, Anderson teaches that the cross-interrogation of the cache block address is accomplished via a directory lookup in the storage control unit (Fig. 1, elements 27-28; column 4, lines 20-27 and 56-62; column 5, lines 45-48).

Regarding claim 12, although the combination of APA, Gaskins, Anderson and Mahalingaiah does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the system of APA, Gaskins, Anderson and Mahalingaiah. The combination of APA, Gaskins, Anderson and Mahalingaiah teaches both a directory and register file. The limitations in claim 12 of the instant application do not define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Gaskins (US 5,930,821) and Anderson (US 3,735,360), and further in view of Mahalingaiah (US

6,073,217) as applied to claim 5 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998).

APA, Gaskins, Anderson and Mahalingaiah are relied upon for the teachings relative to claim 5 as above.

Anderson further teaches an existing cache handling requirement whereby entries in the cache are replaced according to a replacement algorithm (Column 9, lines 33-39).

The combination of APA, Gaskins, Anderson and Mahalingaiah does not teach that the replacement algorithm is a least-recently used replacement algorithm as required by claim 10.

Handy teaches a least recently used cache block replacement algorithm used to determine where to place new blocks of data in a cache (Page 57, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy, in the system made obvious by the combination of APA, Gaskins Anderson and Mahalingaiah, for the purpose of determining where to place new blocks of data in the cache as taught by Handy.

8. Claims 18 is rejected under 35 U.S.C. 103(a) as being anticipated by Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821).

As in claim 18, APA discloses a conventional multi-processor computer system comprising a plurality of central processing units each including an execution unit, an instruction unit, and a plurality of caches including separate instruction and operand caches, where the central processing units are connected to a shared main memory through a storage controller (Page 1, lines 5-22). It is readily apparent in APA that the instruction cache stores instructions that are fetched by the instruction unit and issued to the execution unit, and that the execution unit accesses operands from the operand cache. Therefore, it may be understood that these elements are all directly or indirectly coupled to one another.

APA does not teach that the instruction and operand cache are subjected to a cache coherency protocol with interlocks on cache block access as required by claim 18.

Gaskins discloses a system supporting self-modifying code in a processor system (Column 9, lines 19-24) where an instruction cache and operand cache are subjected to a cache coherency protocol with interlocks on cache block access (Column 3, lines 50-53; Figs. 7 and 8; column 7, lines 60-62; column 8, lines 56-58).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to subject the instruction cache and operand cache to a cache coherency protocol as taught by Gaskins, in the system of APA, in order to support self-modifying code as taught by Gaskins.

9. Claims 19-21, 23 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821) as applied to claim 18 above, and in further view of Anderson (US 3,735,360).

APA and Gaskins are relied upon for the teachings relative to claim 18 as above.

The combination of APA and Gaskins as applied in the rejection of claim 18 above does not teach the limitations required by claims 19-21, 23 and 31-35, however it is noted that these claims are similar to claims 1-4 and 13-17, which are rejected over the combination of APA, Gaskins and Anderson.

Therefore, claim 19 is rejected using the same rationale as for the rejection of claim above.

Claims 20-21 and 23 are rejected using the same rationale as for the rejection of claims 2-4 above.

Claims 31-35 are rejected using the same rationale as for the rejection of claims 13-17 above.

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10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821) and Anderson (US 3,735,360) as applied to claim 21 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998).

APA, Gaskins and Anderson are relied upon for the teachings relative to claim 21 as above.

The combination of APA, Gaskins and Anderson as applied in the rejection of claim 21 above does not teach the limitations required by claim 22, however it is noted that this claim is similar to claim 10, which is rejected over the combination of APA, Gaskins, Anderson and Handy.

Therefore, claim 22 is rejected using the same rationale as for the rejection of claim 10 above.

11. Claims 24-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Gaskins (US 5,930,821), Anderson (US 3,735,360) and Handy (The Cache Memory Book, Jim Handy, 1998) as applied to claim 22 above, and further in view of Mahalingaiah (US 6,073,217).

The combination of APA, Gaskins, Anderson and Handy as applied in the rejection of claim 22 above does not teach the limitations required by claims 24-26 and 28-30, however it is noted that these claims are similar to claims 5-7, 9 and 11-12, which are rejected over the combination of APA, Gaskins, Anderson and Mahalingaiah.

Therefore, claims 24-26 are rejected using the same rationale as for the rejection of claims 5-7 above.

Claim 28 is rejected using the same rationale as for the rejection of claim 9 above.

Claims 29-30 are rejected using the same rationale as for the rejection of claim 11-12 above.

Response to Arguments

12. Applicant's arguments filed 8 July 2004 with respect to the rejection of claims 1-7, 9-26 and 28-35 under 35 USC 102(b) have been fully considered but they are not persuasive.

With regard to the rejection of claims 1-4 and 13-17, applicant contends that the cache coherency protocol disclosed by Anderson is applied to data sharing between two processors, and that there is no teaching with regard to an application to instructions that later modify themselves. Applicant further contends that Gaskins includes no teaching with respect to cache coherency with storage controller and multiple processors. Finally, Applicant contends that

because neither the admitted prior art (APA), Gaskins nor Anderson disclose or teach an element of the invention they cannot render the claims unpatentable (Amdt. B, page 13, paragraph 2).

In response to Applicant's arguments, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. The test for obviousness is not whether the claimed invention is expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Further regarding the rejection of claims 1-4 and 13-17, Applicant maintains that improper hindsight has been used because no motivation for combining the references has been given. Applicant also asserts that if such a motivation did exist, the Gaskins reference would have disclosed the claimed configuration (Amdt. B, page 14, paragraphs 2 and 3).

In response to Applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Furthermore, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the motivation for combining APA and Gaskins as stated in the prior office action and restated above, is to incorporate the advantageous support for self-modifying code taught by Gaskins in the system of APA. The motivation for combining Anderson with APA and Gaskins as stated in the prior office action and restated above, is derived from the similar nature of the problems to be solved. The combination of APA and Gaskins comprises a cache coherency protocol for a pair of parallel caches sharing a common main storage. Anderson teaches a cache coherency protocol that addresses the same problem found in APA and Gaskins, which would lead a person of ordinary skill in the art to consider the teachings of Anderson as a possible solution to the problem in APA and Gaskins, and apply their teachings together. See MPEP § 2143.01.

Applicant's argument contending that if such a motivation did exist, the Gaskins reference would have disclosed the claimed configuration is not persuasive. What Gaskins has not disclosed is irrelevant. The combination of the prior art references teaches all of the claim limitations, and a motivation for the combination has been given as above. See MPEP § 2143.

Regarding the rejection of claims 5-7, 9, 11-12, 28 and 29-30, Applicant contends that there improper hindsight has been used and that no motivation to combine Mahalingaiah with APA, Gaskins and Anderson has been given. Applicant further asserts that if such motivation did exist, Gaskins and/or Mahalingaiah would have disclosed the claimed configuration (Amdt. B, page 17, paragraph 2).

In response to Applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, Applicant is referred to Examiner's comments on this subject with regard to the rejection of claims 1-4 and 13-17 as above.

Regarding the motivation to combine the references, in this case the motivation to combine Mahalingaiah with APA, Gaskins and Anderson as stated in the prior office action and restated above, is to allow the correct execution of self-modifying code as taught by Mahalingaiah.

Applicant's argument contending that if such a motivation did exist, the Gaskins and/or Mahalingaiah references would have disclosed the claimed configuration is not persuasive. Applicant is referred to Examiner's comments regarding this line of reasoning with regard to the rejection of claims 1-4 and 13-17 as above.

Applicant's arguments in response to the rejection of claim 10 make similar assertions regarding improper hindsight reasoning, lack of a motivation to combine the references, and what the cited references would have disclosed if such a motivation did exist (Amdt. B, page 18).

Applicant is again referred to Examiner's comments above with regard to these arguments and lines of reasoning, noting that the motivation to combine Handy with APA, Gaskins, Anderson and Mahalingaiah as stated in the prior office action and restated above, is for determining where to place new blocks of data in the cache as taught by Handy.

Applicant's arguments in response to the rejection of claims 18-35 are not persuasive for the same reasons given above.

Allowable Subject Matter

13. Claims 8 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, following correction of all other outstanding objections.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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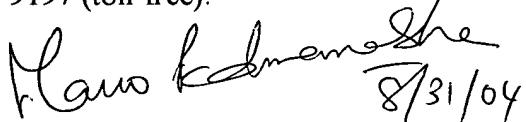
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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